

# VJ 10/800377



### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Cho et al

Attorney Docket No.: NOVLP089/NVLS-2887

Patent No.: 7,265,061 B1

Issued: September 4, 2007

Title: Method and Apparatus for UV Exposure of Low Dielectric Constant Materials for Porogen Removal and Improved Mechanical Properties

**CERTIFICATE OF MAILING** 

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on September 9, 2008 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

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Ouyen Vuong

## REQUEST FOR CERTIFICATE OF CORRECTION OF APPLICANT'S MISTAKE (35 U.S.C §255, 37 C.F.R. §1.323)

Certificate

SEP 1 6 2008

of Correction

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing.

A mistake of a clerical or typographical nature, or minor in character appears in the above-referenced patent; however, the mistake occurred in good faith. The correction introduces no new matter nor requires reexamination. The mistake occurred because of a typographical error.

The errors together with the exact page and line number where the errors appear in the application file are as follows:

03/10/2003 NATERENI 62800397 7255551

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103,08 02

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(Also Form PT-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,265,061 B1

DATED : September 4, 2007 Page 1 of 1

INVENTOR(S): Cho et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

#### In the Claims:

Column 14, line 61, change "2230 W/cm2" to --2230 mW/cm2--

Column 14, line 61 change "3118 W/cm2" to -- 3118 mW/cm2 --

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PATENT NO. 7,265,061 B1

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Denise S. Bergin WEAVER AUSTIN VILLENEUVE & SAMPSON LLP P.O. Box 70250 Oakland, CA 94612-0250

SEP 1 2 1008. US

CLAIMS:

- 1. In line 12 of claim 1 (column 14, line 61) change "2230 W/cm2" to --2230 mW/cm2--. This error appears in the Response to Notice of Non- Compliant Amendment as filed on September 13, 2006, on page 2, line 12. This appears correctly in the application as filed on March 11, 2004, on page 14, line 9.
- 2. In line 12 of claim 1 (column 14, line 61) change "3118 W/cm²" to --3118 mW/cm²--. This error appears in the Response to Notice of Non- Compliant Amendment as filed on September 13, 2006, on page 2, line 12. This appears correctly in the application as filed on March 11, 2004, on page 14, line 9.

Check No. \_\_\_\_\_ in the amount of \$100.00 is enclosed in accordance with 37 CFR § 1.20(a). However, if it is determined that any additional fees are due the Commissioner is hereby authorized to charge such fees to Deposit Account 504480 (Order No. NOVLP089/NVLS-2887).

Respectfully submitted, Weaver Austin Villeneuve & Sampson LLP

Denise S. Bergin

Registration No. 50,581

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P.O. Box 70250 Oakland, CA 94612-0250 510-663-1100 wafer was modulated by adjusting the distance between the wafer substrate and the UV source.

As shown by Figure 2B, increasing UV exposure time increased film hardnesses and k-values using both UV power densities (2230 mW/cm<sup>2</sup> and 3118 mW/cm<sup>2</sup>). As illustrated by the best-fit curves, in general, hardness values and k-values increased more quickly with increased exposure time using the higher power density light. Thus, those samples exposed to the lower power densities will require longer exposure times than those samples exposed to the higher power densities to achieve the desired hardness. For example, wafer sample 207, which is exposed to the lower power density (2230 mW/cm<sup>2</sup>), was exposed for about 700 seconds to achieve a hardness value of about 1.4 GPa, while wafer sample 209, which is exposed to the higher power density (3118 mW/cm<sup>2</sup>), was only exposed for about 200 seconds to achieve about the same hardness value (about 1.4 GPa). Note although the hardness values for wafer samples 207 and 209 are about equivalent, the k-values differ somewhat (k for 207 is about 2.4, k for 209 is about 2.7). Note that for many ultra low-k dielectric applications, an acceptable hardness value is about 1.2 GPa or above. Thus, for those samples exposed to 3118 mW/cm<sup>2</sup>, exposure times of about 150 seconds (indicated by 211 area) and above and for those samples exposed to 2230 mW/cm<sup>2</sup>, exposure times of about 400 seconds (indicated by 213 area) and above are preferred. Of course, for any particular application, the exposure times and UV power densities will vary depending upon a multitude of factors including film type, film thickness, application type, desired film properties, apparatus configuration and other factors.

The wafer substrate temperature may influence the hardening process. In some embodiments, higher temperatures may be more effective, but the temperature should not be too high as to cause damage to the substrate device. In general, temperatures below about 450 degrees C are preferable, more preferably  $\leq 400$  degrees C, as higher temperatures can damage a partially fabricated device, particularly one that employs copper lines. Typical temperatures range between about -10 up to 450 degrees C. It should be noted that exposure to UV radiation can itself contribute to substrate heating.

Note that the operations 103 and 105 can be conducted in a single vessel or in two separate vessels, one for UV exposure for removing porogen and another for UV exposure for mechanical hardening. In preferred embodiments, the two operations are performed in the same reaction chamber. An example of a suitable apparatus for accomplishing this will be described later. If the operations are performed in the same reaction chamber, it is possible to overlap some portions of the operation. For example, a light source that can

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This listing of claims will replace all prior versions, and listings, of claims in the application:

#### **Listing of Claims**

- 1. (Currently Amended) A method of preparing a porous low-k dielectric layer on a substrate, the method comprising:
- (a) forming a precursor film on the substrate, the precursor film comprising a porogen and a structure former;
- (b) removing the porogen from the precursor film to thereby create voids within the dielectric material and form the porous low-k dielectric layer; and
- (c) exposing the dielectric material to ultraviolet radiation in a manner that increases the mechanical strength of the porous low-k dielectric layer; wherein the ultraviolet radiation in (c) has an intensity of between about 2230 W/cm<sup>2</sup> and 3118 W/cm<sup>2</sup> and (c) occurs for a time period time period between about 1 and 200 seconds.
  - 2. (Original) The method of claim 1, wherein the substrate is a semiconductor wafer.
- 3. (Original) The method of claim 2, wherein the porous low-k dielectric layer is formed on the semiconductor wafer using a single-wafer or batch process.
- 4. (Original) The method of claim 1, wherein the precursor film comprises a porogen and a silicon-containing structure former.
- 5. (Original) The method of claim 1, wherein the precursor film is formed by codepositing the porogen with the structure former.
- 6. (Original) The method of claim 1, wherein the structure former is produced from at least one of a silane, an alkylsilane, an alkoxysilane, siloxane, carbon-doped variation thereof, or combination thereof.
- 7. (Original) The method of claim 1, wherein the structure former is produced from diethoxymethylsilane (DEMS), octamethylcyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TMCTS), dimethyldimethoxysilane (DMDMOS), carbon-doped oxides or a combination thereof.
- 8. (Original) The method of claim 1, wherein the porogen comprises a polyfunctional cyclic non-aromatic compound.